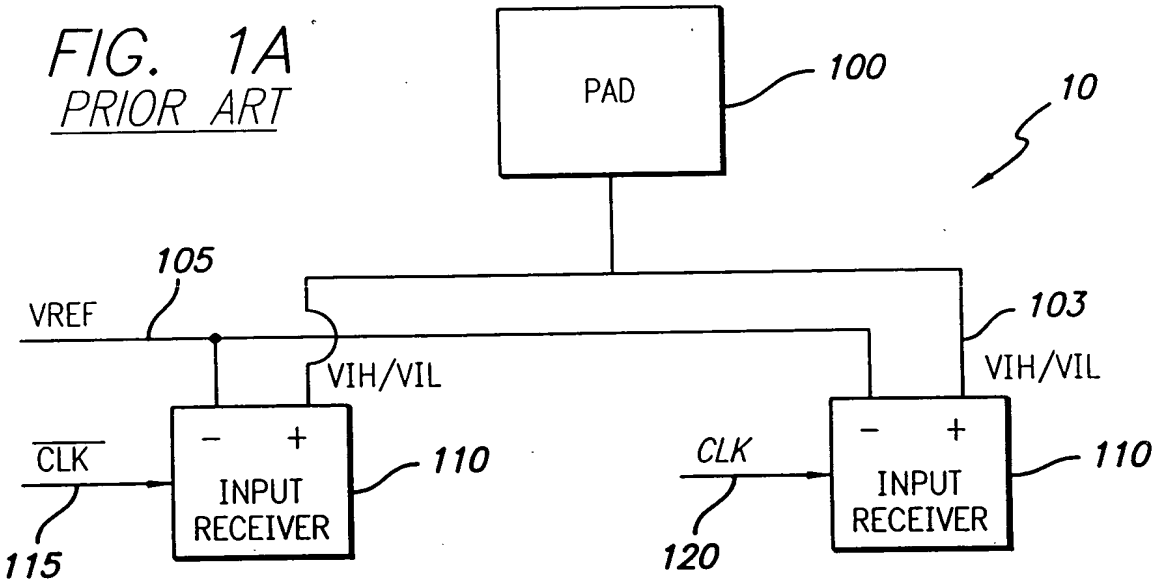
FIG. 1A
PRIOR ART



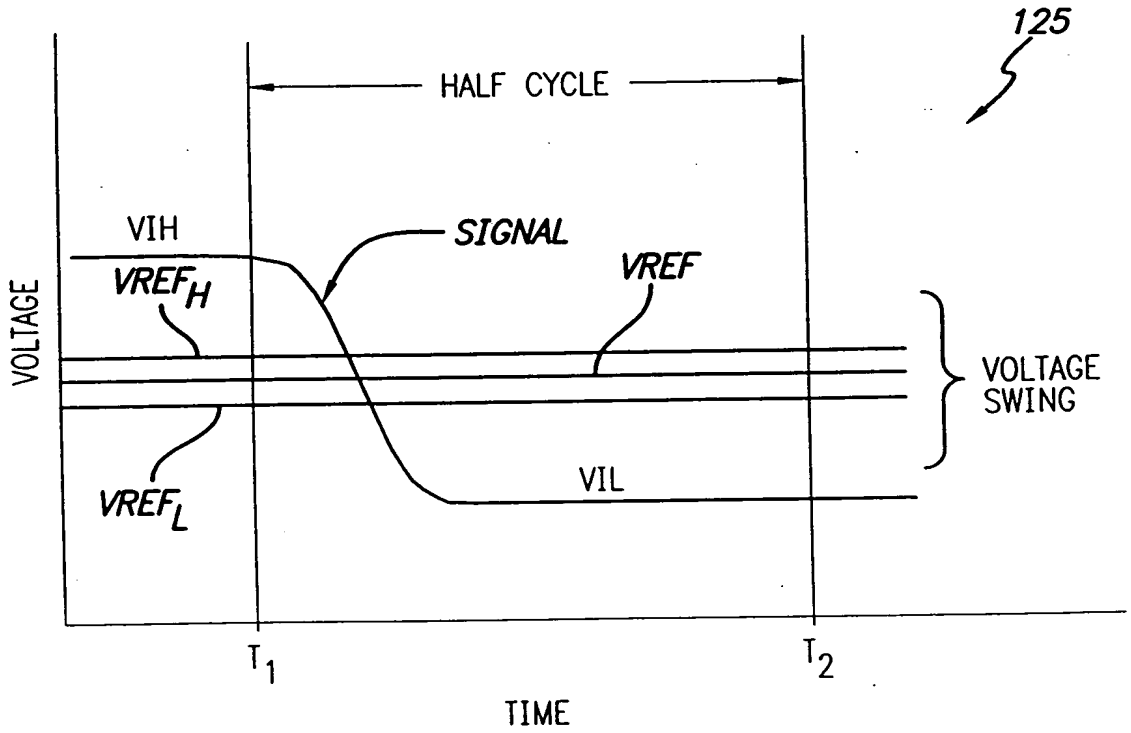
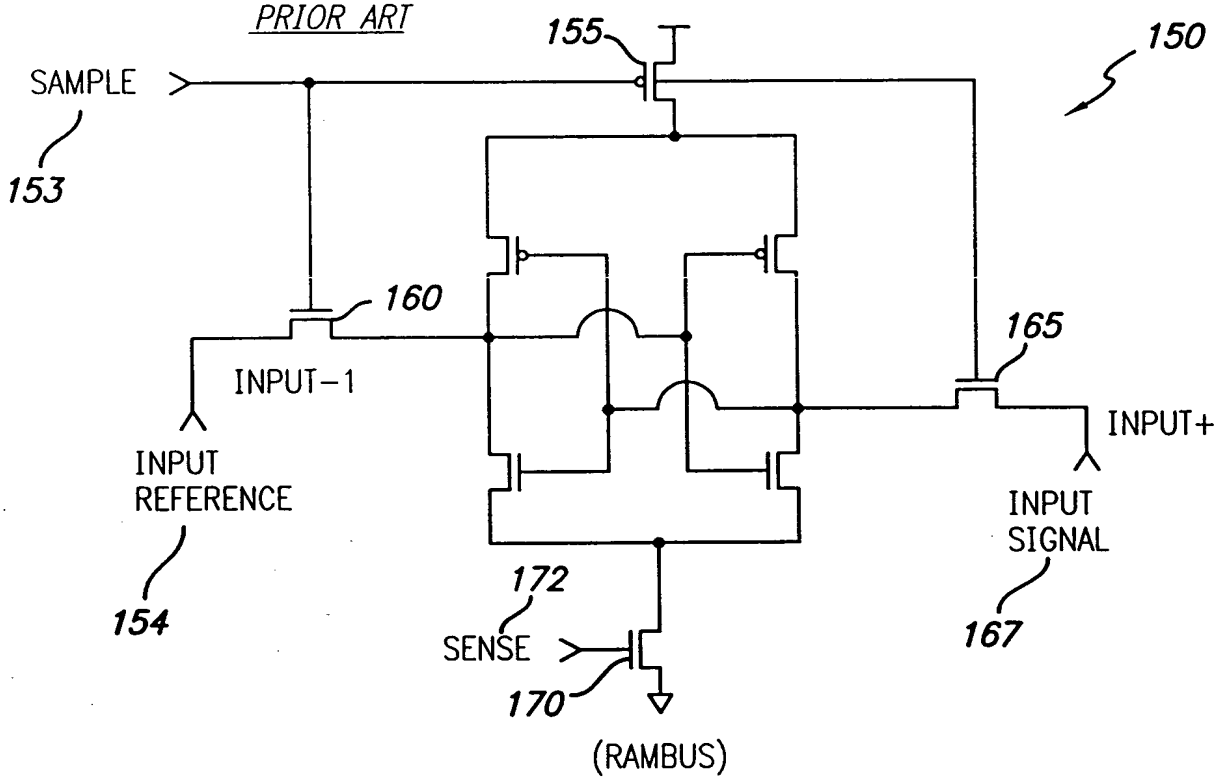


FIG. 1B
PRIOR ART

FIG. 1C

PRIOR ART



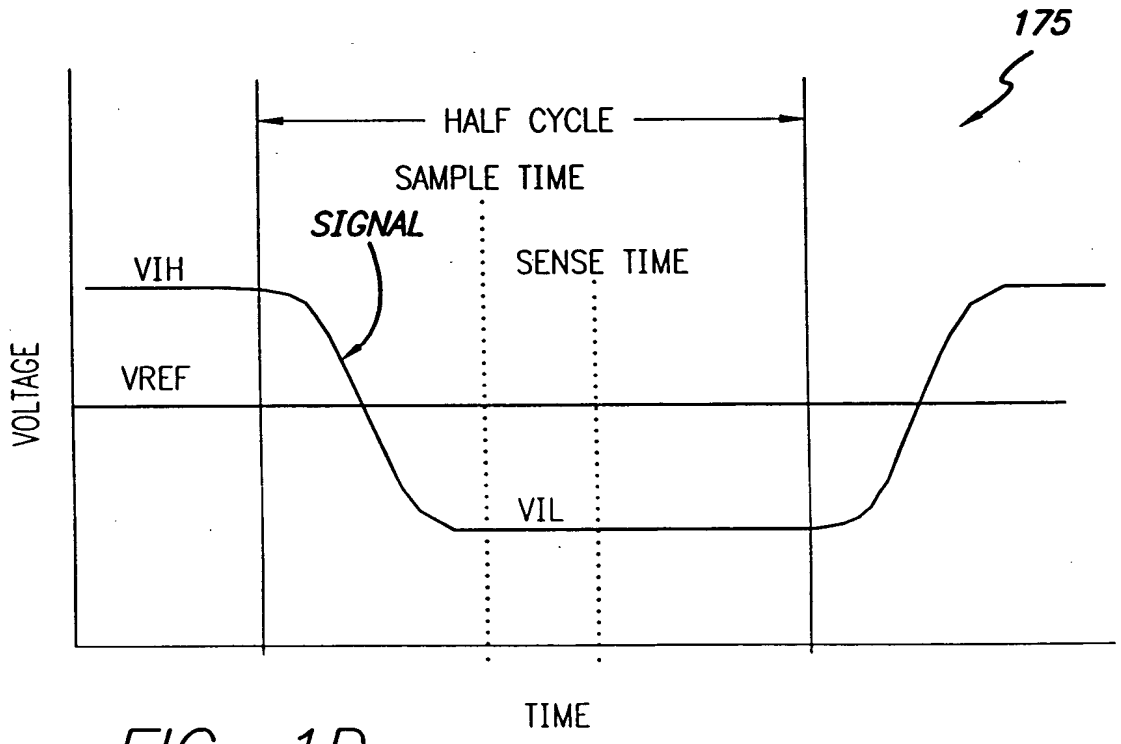


FIG. 1D

PRIOR ART

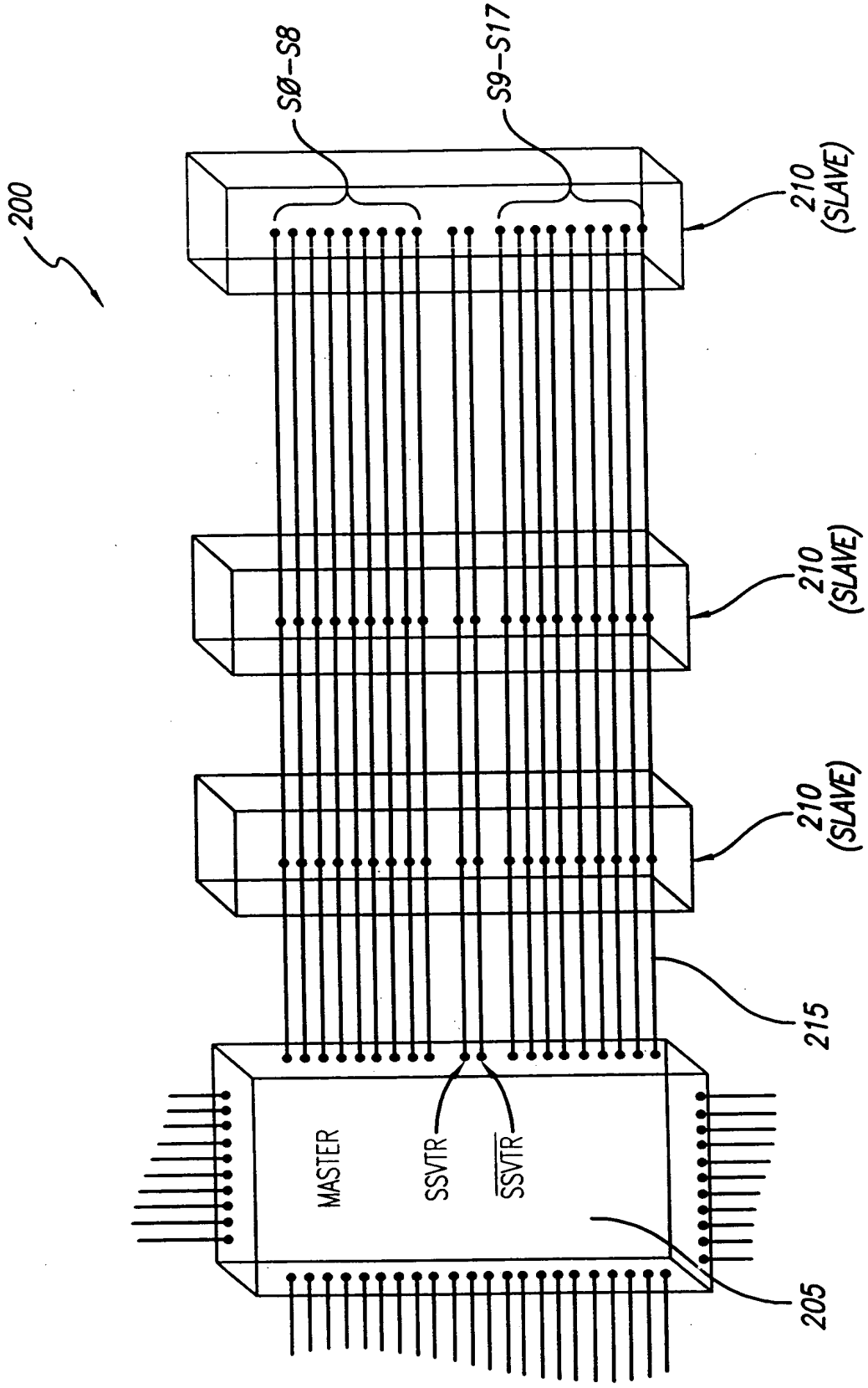

200
S0–S8
S9–S17
210
(SLAVE)
210
(SLAVE)
210
(SLAVE)
215
MASTER
SSVTR
$\overline{SSVTR}$
205

FIG. 2A

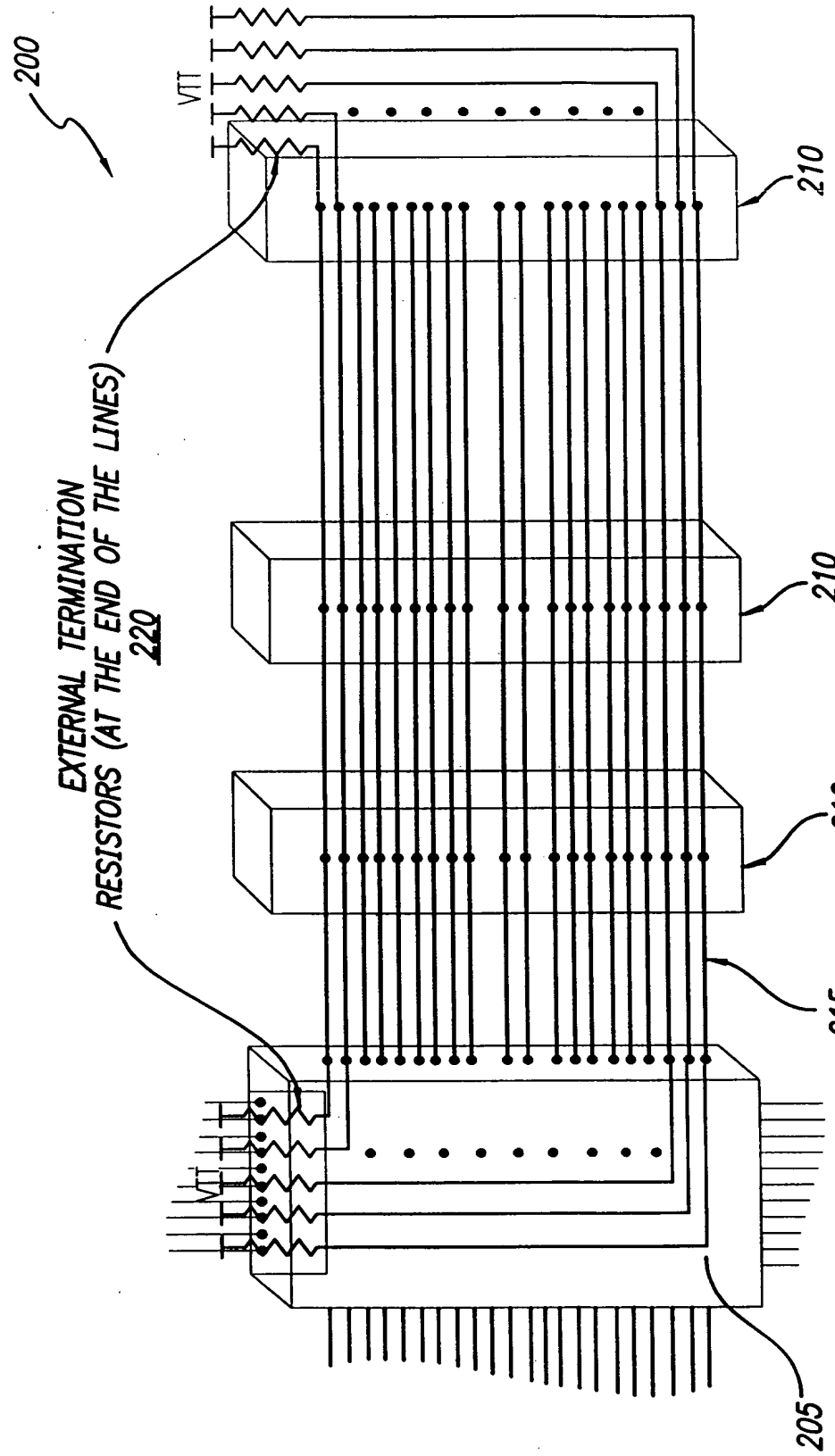

200
VTT
210
210
210
EXTERNAL TERMINATION
RESISTORS (AT THE END OF THE LINES)
220
215
VTT
205

FIG. 2B

FIG. 3A

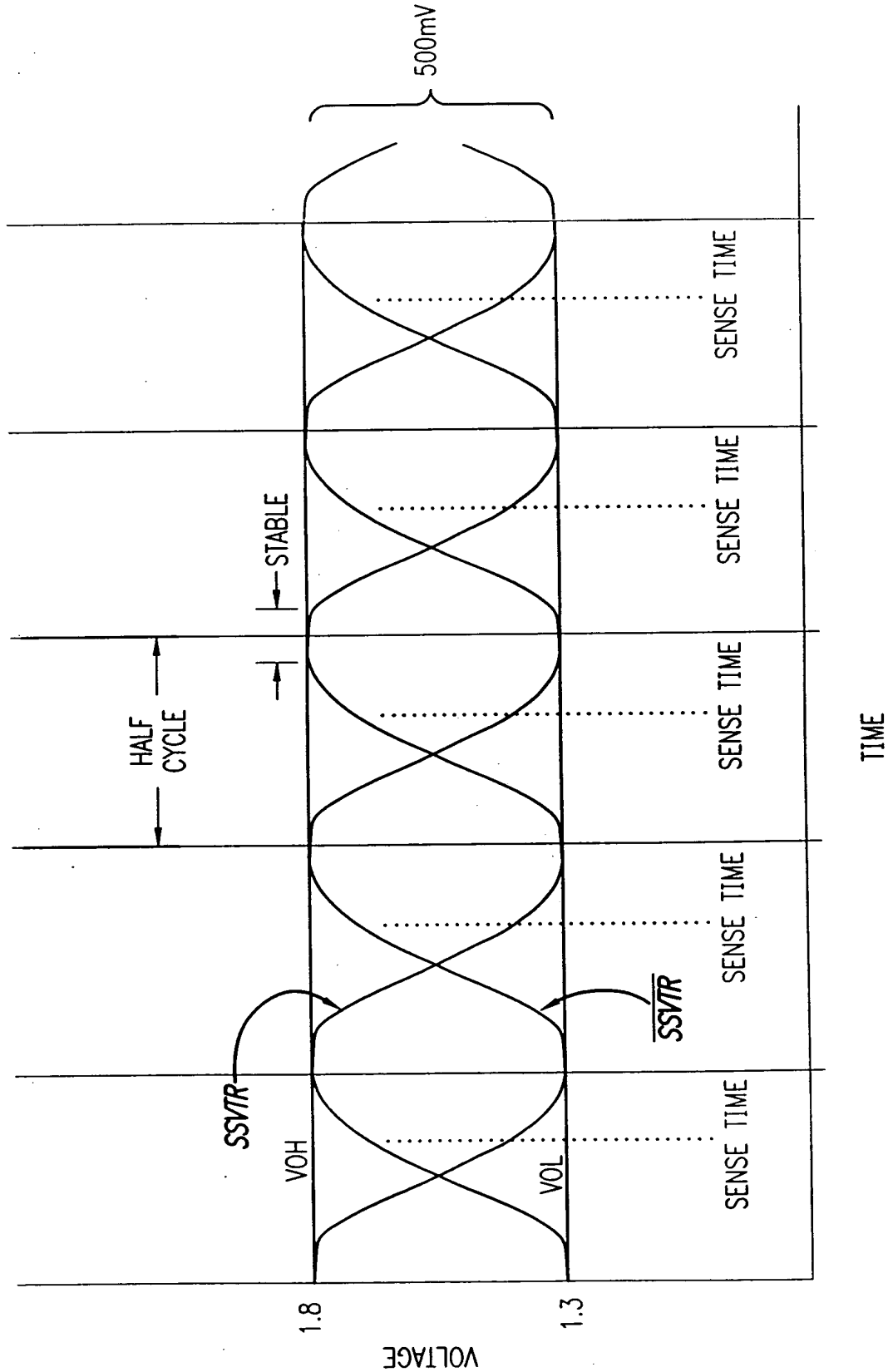

500mV
SENSE TIME
SENSE TIME
SENSE TIME
SENSE TIME
SENSE TIME
STABLE
HALF CYCLE
SSVTR
SSVTR
VOH
VOL
1.8
1.3
VOLTAGE
TIME

FIG. 3B

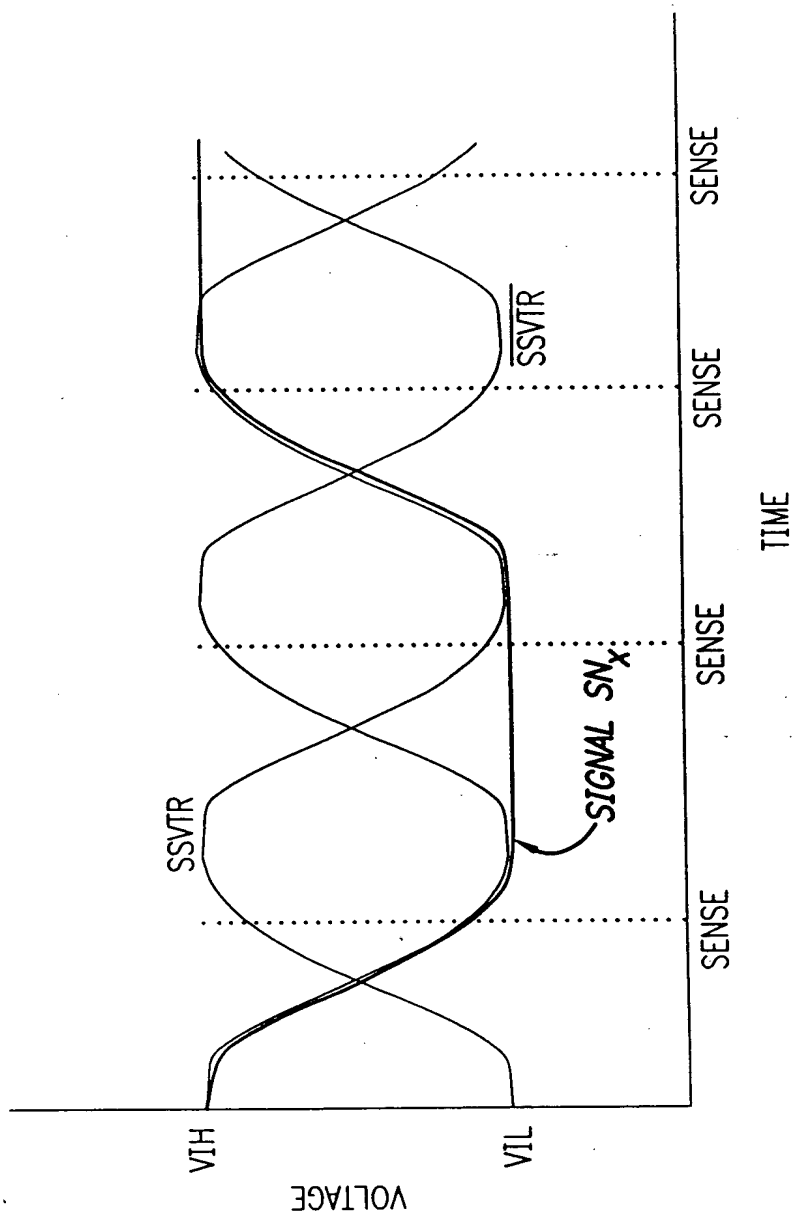

SENSE
SENSE
SENSE
SENSE
TIME
SSVTR
SSVTR
SIGNAL SN_x
VIH
VIL
VOLTAGE

FIG. 4-1

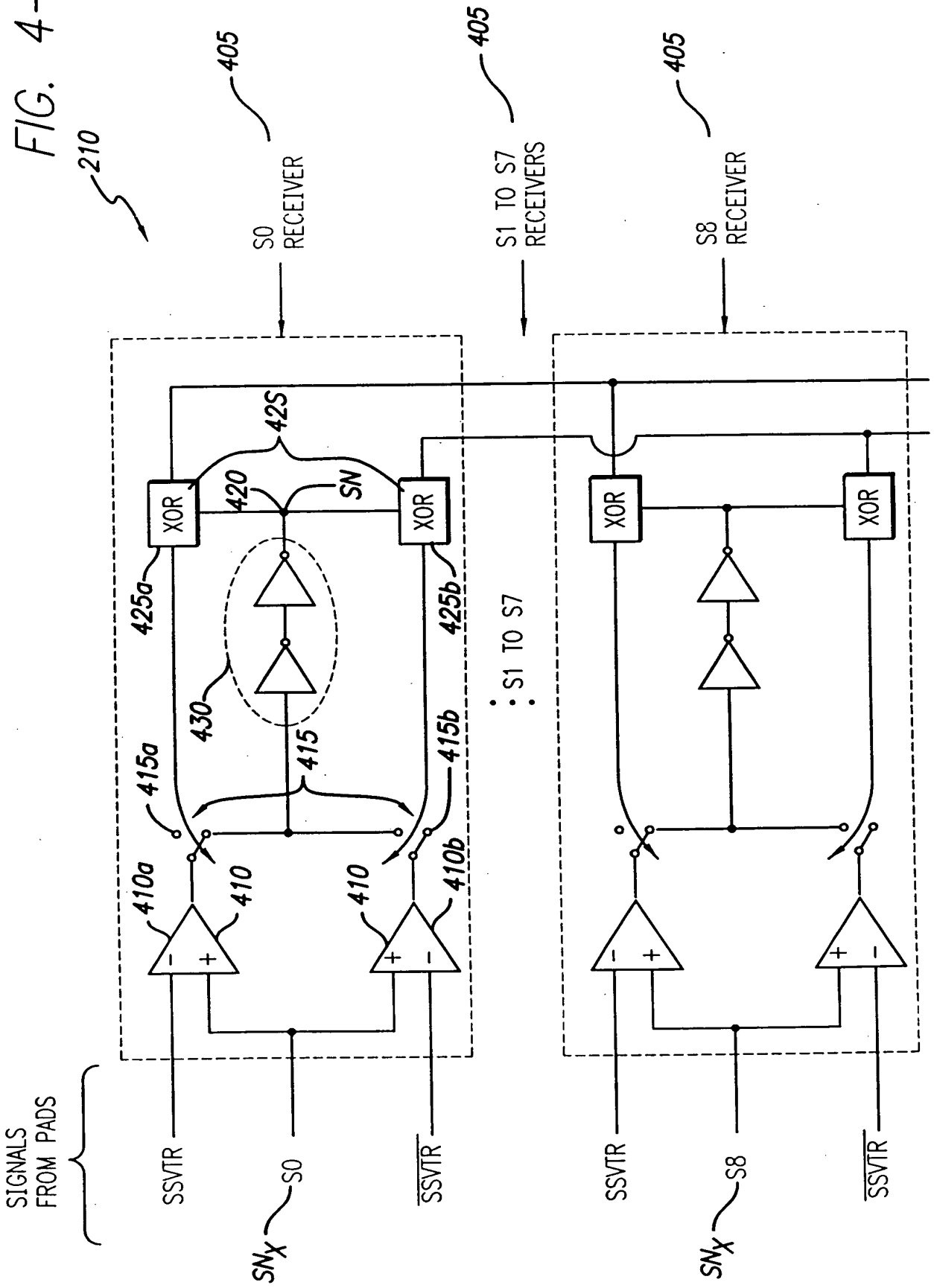

210
405
S0 RECEIVER
405
S1 TO S7 RECEIVERS
405
S8 RECEIVER
XOR
XOR
XOR
XOR
420
SN
425a
425b
430
415
415a
415b
410a
410
410
410b
S1 TO S7
SIGNALS FROM PADS
SSVTR
S0
SNX
SSVTR
SSVTR
S8
SNX
SSVTR

FIG. 4-2

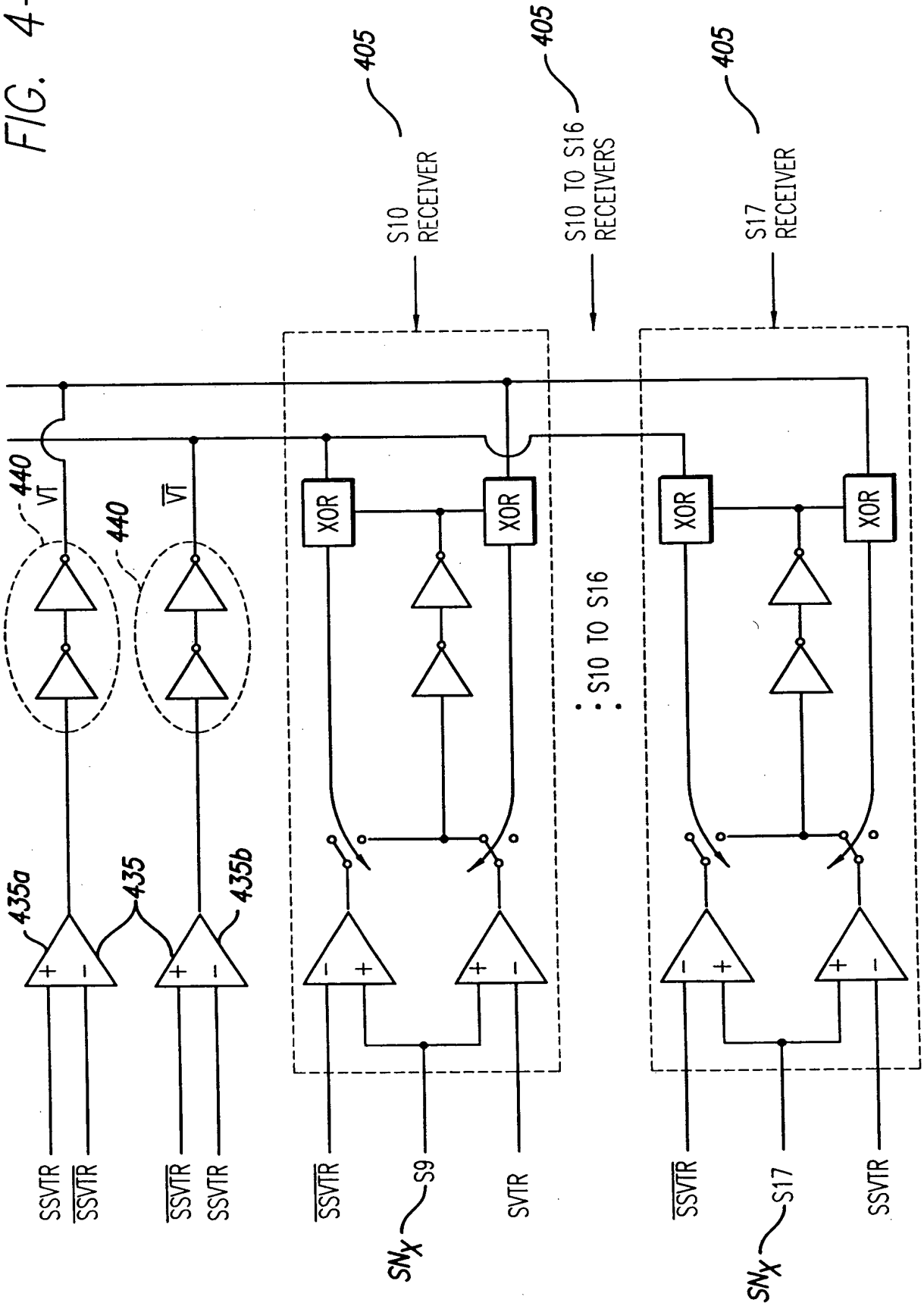
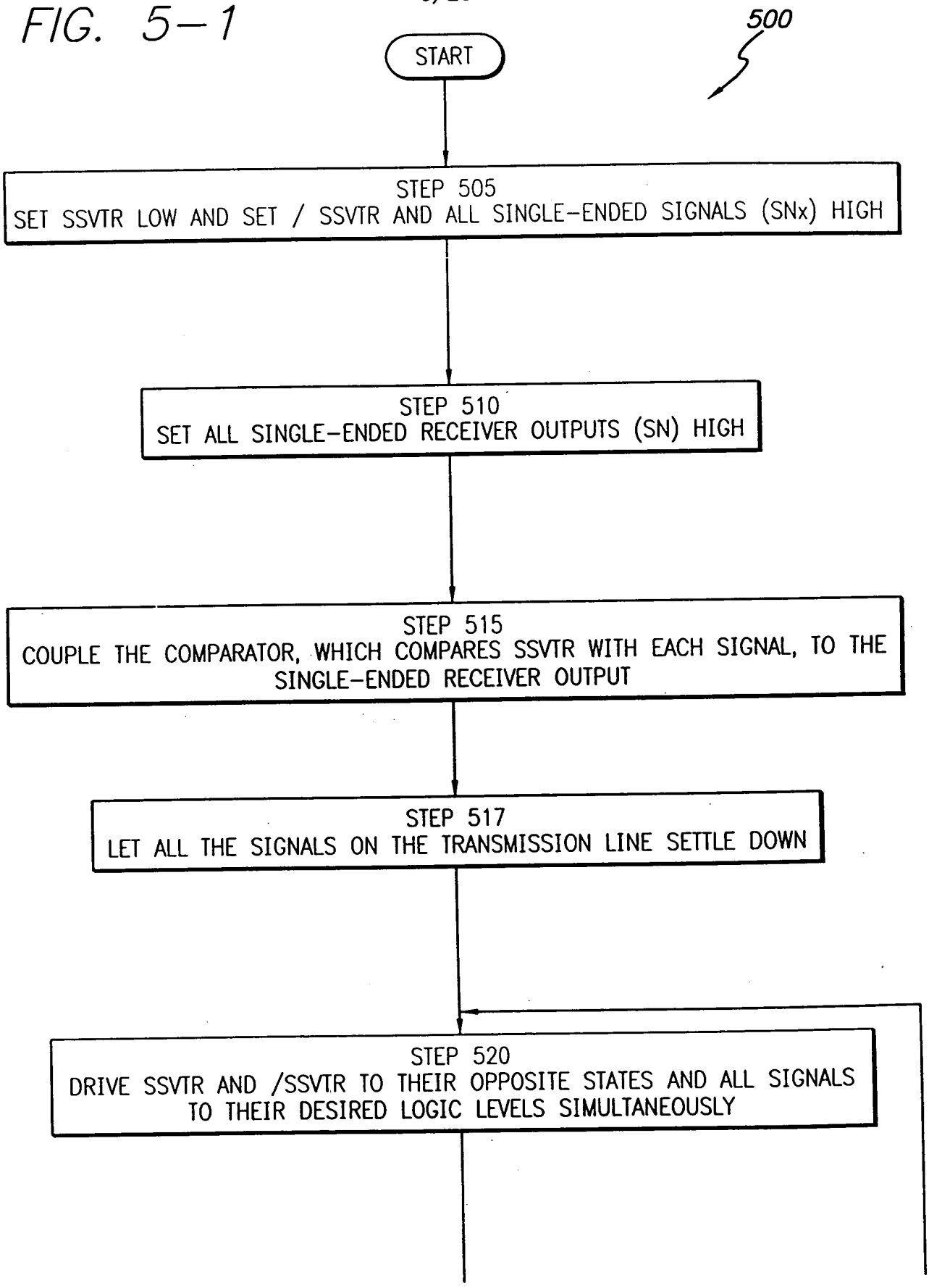

405
S10 RECEIVER
405
S10 TO S16 RECEIVERS
405
S17 RECEIVER
440
VT
440
$\overline{VT}$
XOR
S10 TO S16
435a
435
435b
SSVTR
$\overline{SSVTR}$
$\overline{SSVTR}$
SSVTR
$\overline{SSVTR}$
S9
SVTR
SN_X
$\overline{SSVTR}$
S17
SSVTR
SN_X

FIG. 5-1


500
START
STEP 505
SET SSVTR LOW AND SET / SSVTR AND ALL SINGLE-ENDED SIGNALS (SNx) HIGH
STEP 510
SET ALL SINGLE-ENDED RECEIVER OUTPUTS (SN) HIGH
STEP 515
COUPLE THE COMPARATOR, WHICH COMPARES SSVTR WITH EACH SIGNAL, TO THE SINGLE-ENDED RECEIVER OUTPUT
STEP 517
LET ALL THE SIGNALS ON THE TRANSMISSION LINE SETTLE DOWN
STEP 520
DRIVE SSVTR AND /SSVTR TO THEIR OPPOSITE STATES AND ALL SIGNALS TO THEIR DESIRED LOGIC LEVELS SIMULTANEOUSLY

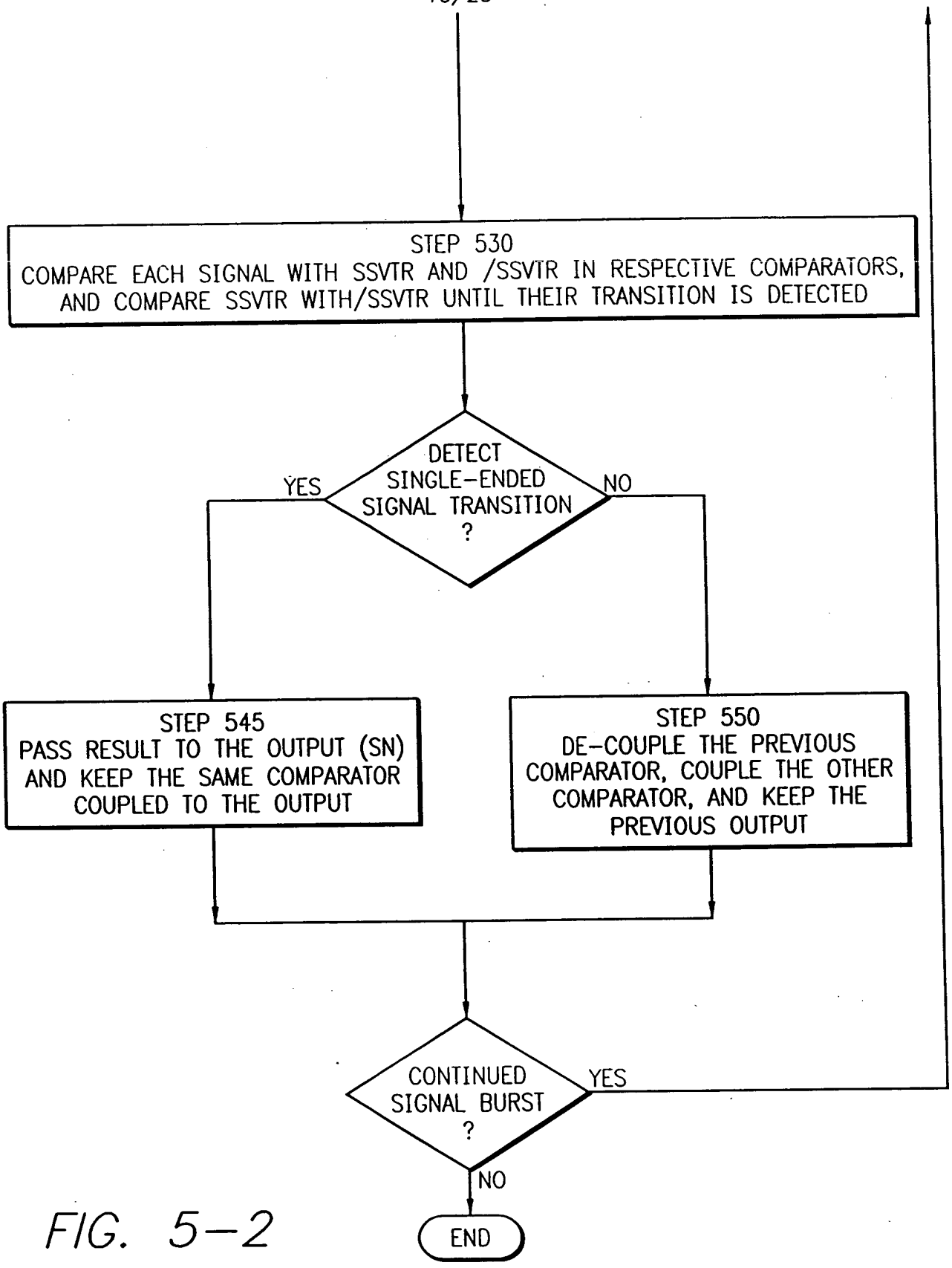

STEP 530
COMPARE EACH SIGNAL WITH SSVTR AND /SSVTR IN RESPECTIVE COMPARATORS, AND COMPARE SSVTR WITH/SSVTR UNTIL THEIR TRANSITION IS DETECTED
DETECT SINGLE-ENDED SIGNAL TRANSITION ?
YES
NO
STEP 545
PASS RESULT TO THE OUTPUT (SN) AND KEEP THE SAME COMPARATOR COUPLED TO THE OUTPUT
STEP 550
DE-COUPLE THE PREVIOUS COMPARATOR, COUPLE THE OTHER COMPARATOR, AND KEEP THE PREVIOUS OUTPUT
CONTINUED SIGNAL BURST ?
YES
NO
END

FIG. 5-2

FIG. 6A

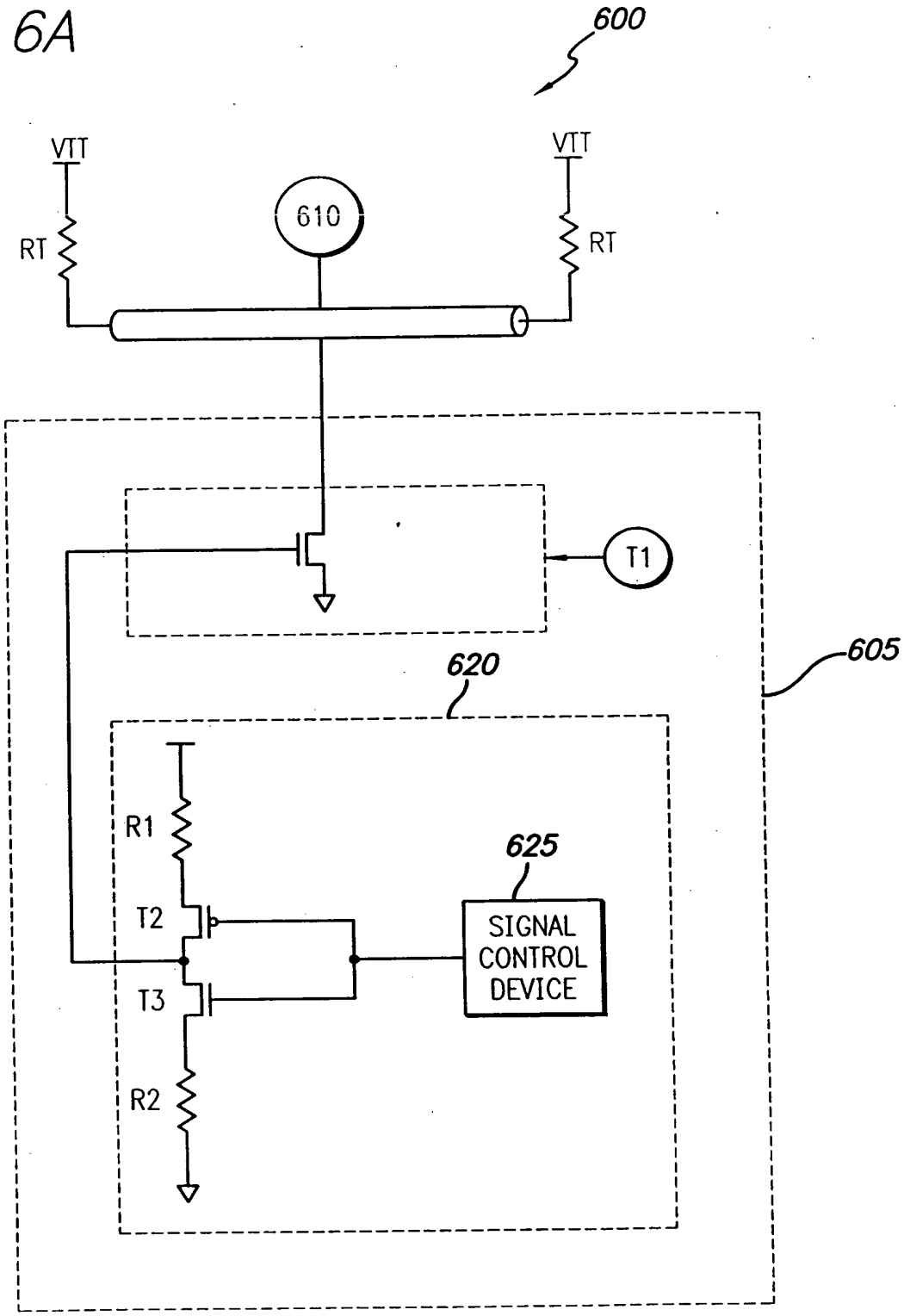

600
VTT
VTT
610
RT
RT
T1
605
620
R1
625
T2
SIGNAL CONTROL DEVICE
T3
R2

FIG. 6B

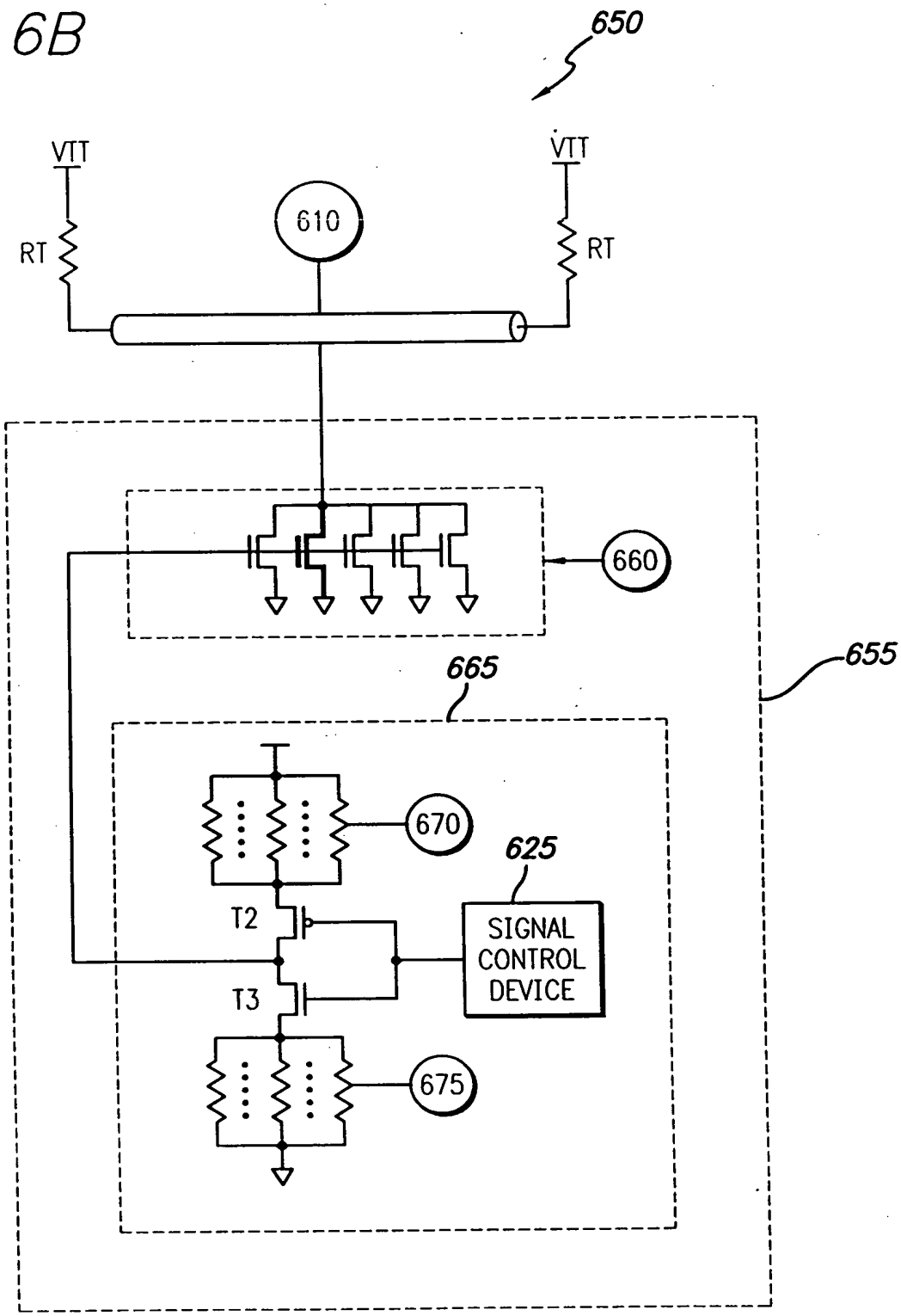

650
VTT
VTT
RT
610
RT
660
655
665
670
625
T2
SIGNAL CONTROL DEVICE
T3
675

FIG. 7A

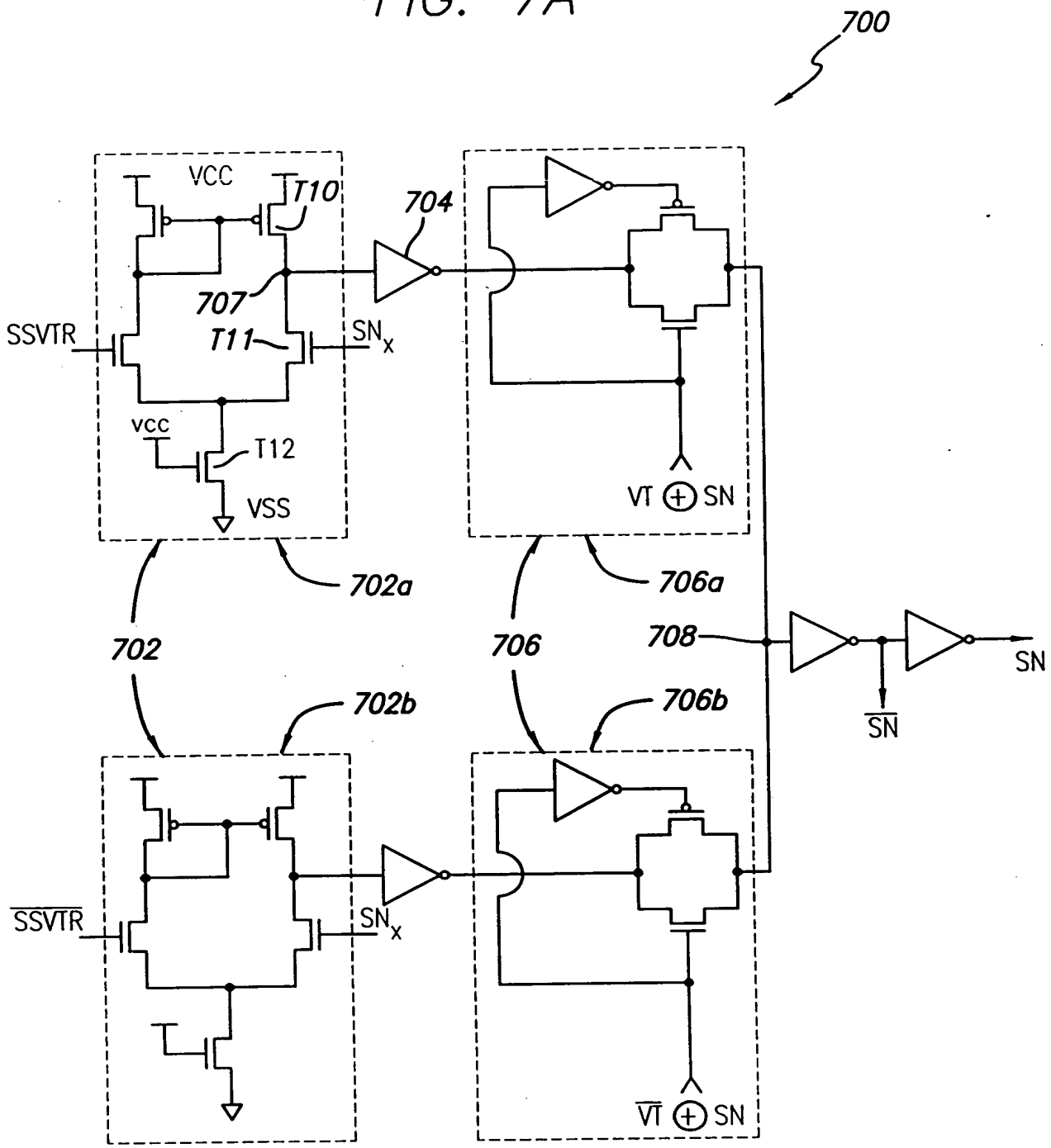

700
VCC
T10
704
707
SSVTR
T11
SNx
VCC
T12
VSS
VT ⊕ SN
702a
706a
702
706
708
SN
SN
702b
706b
SSVTR
SNx
VT ⊕ SN

FIG. 7B

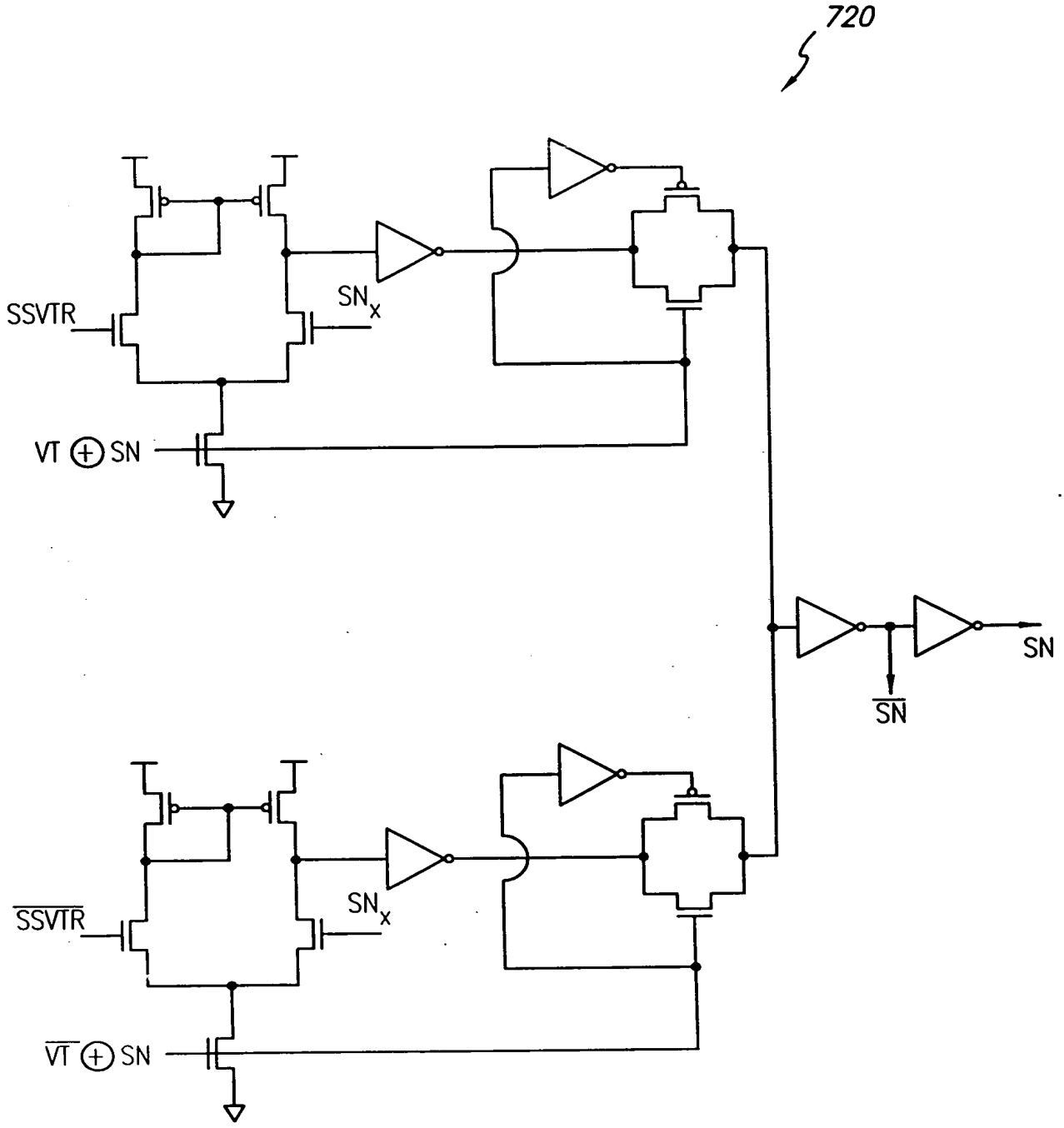


FIG. 7C

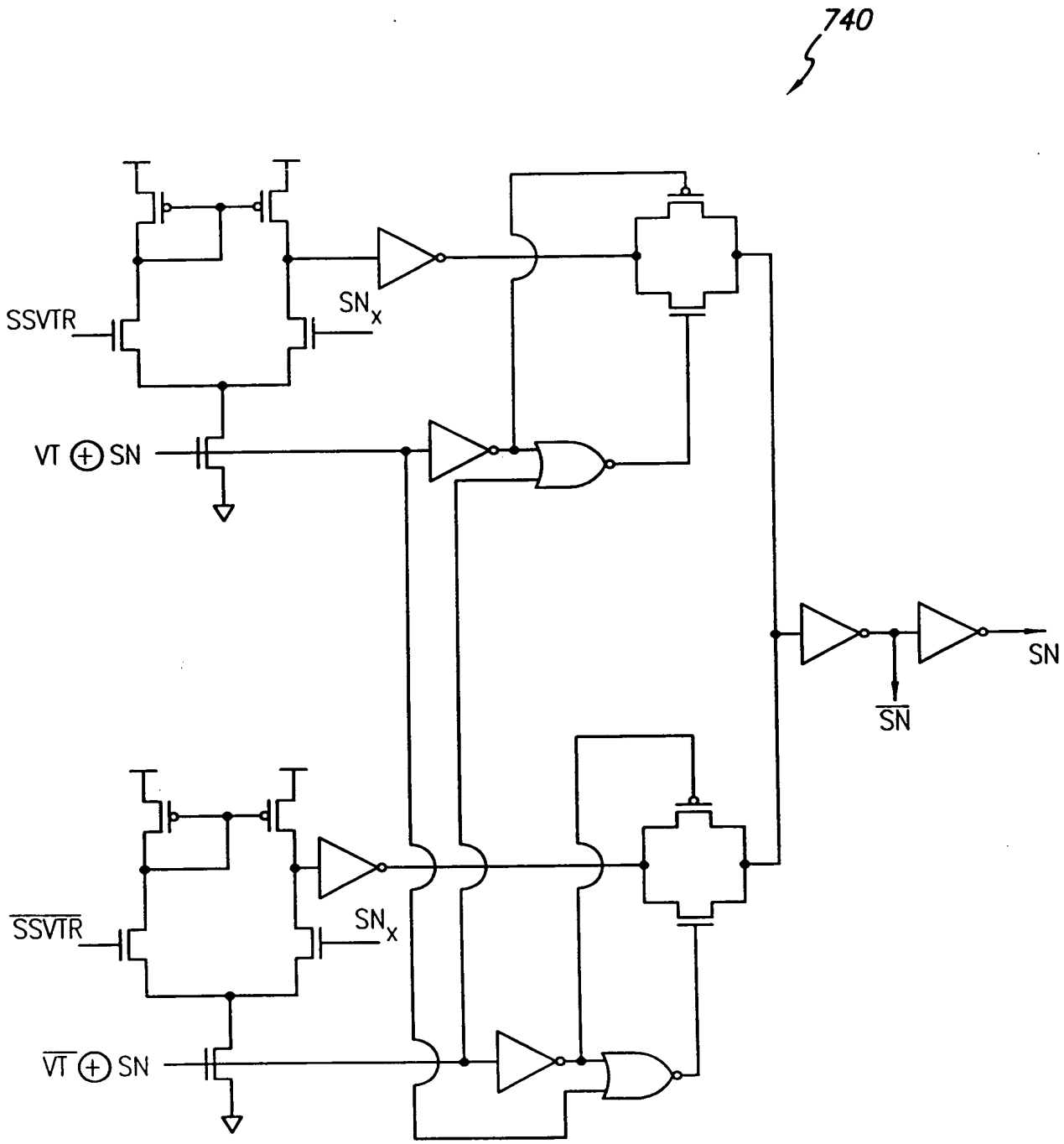


FIG. 7D

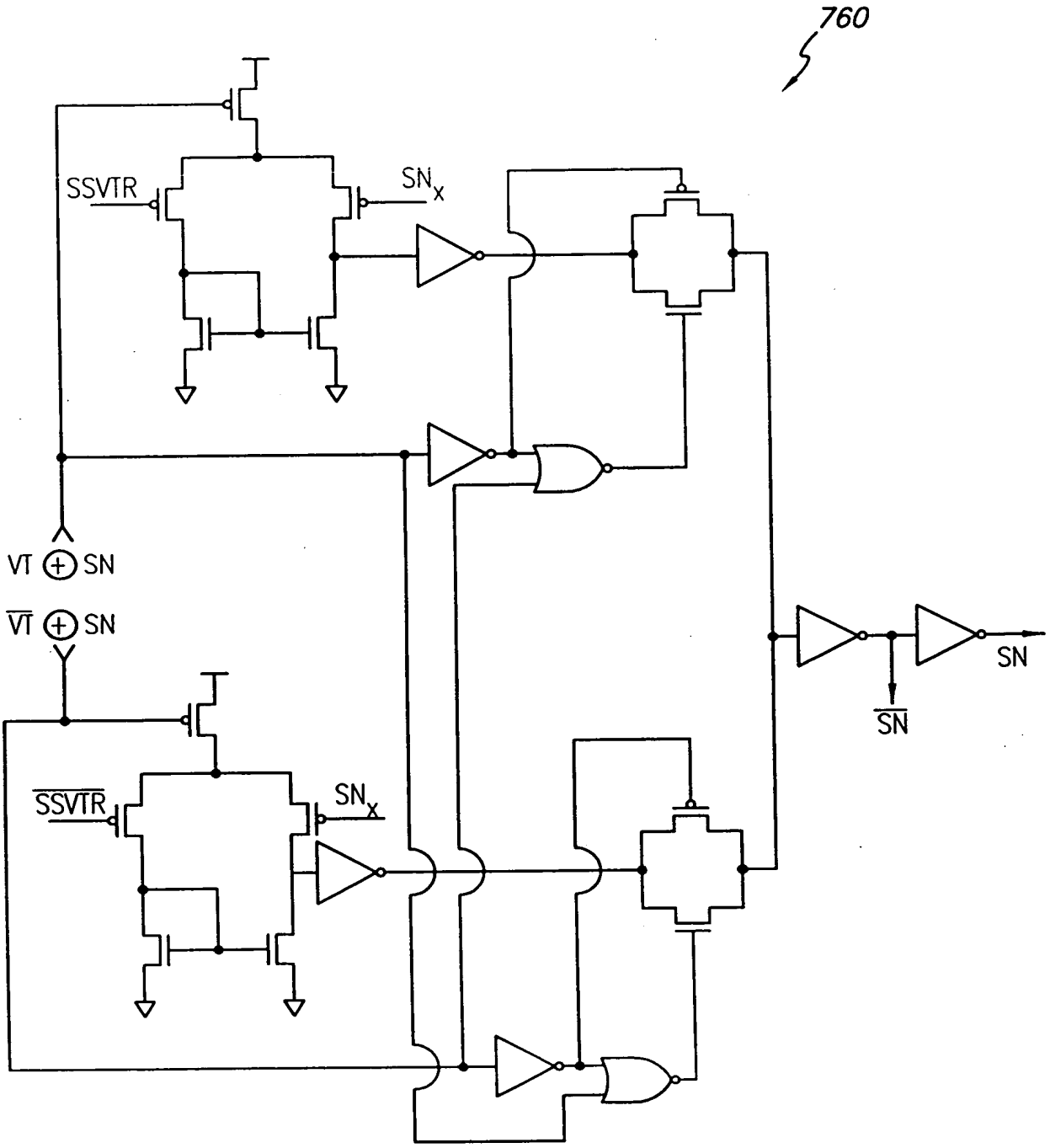


FIG. 8A

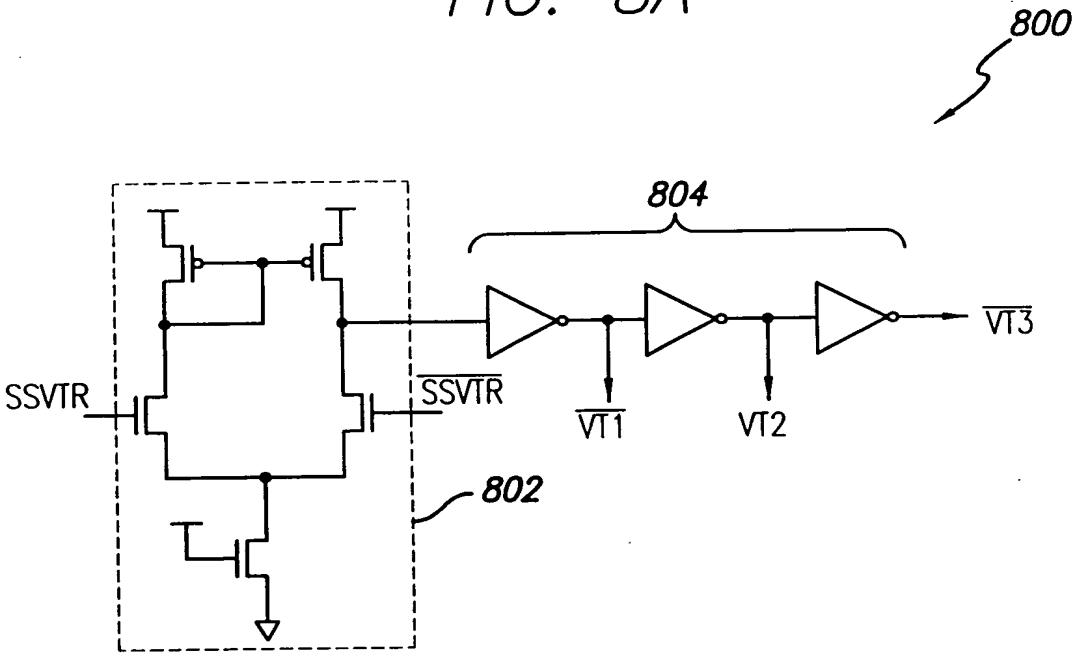

800
804
SSVTR
SSVTR
VT1
VT2
VT3
802

FIG. 8B

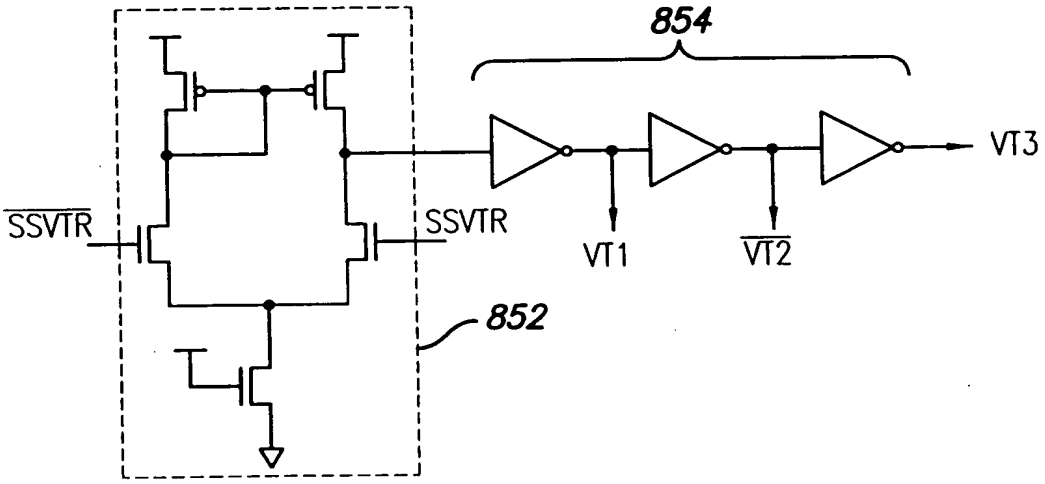

850
854
SSVTR
SSVTR
VT1
VT2
VT3
852

FIG. 9-1

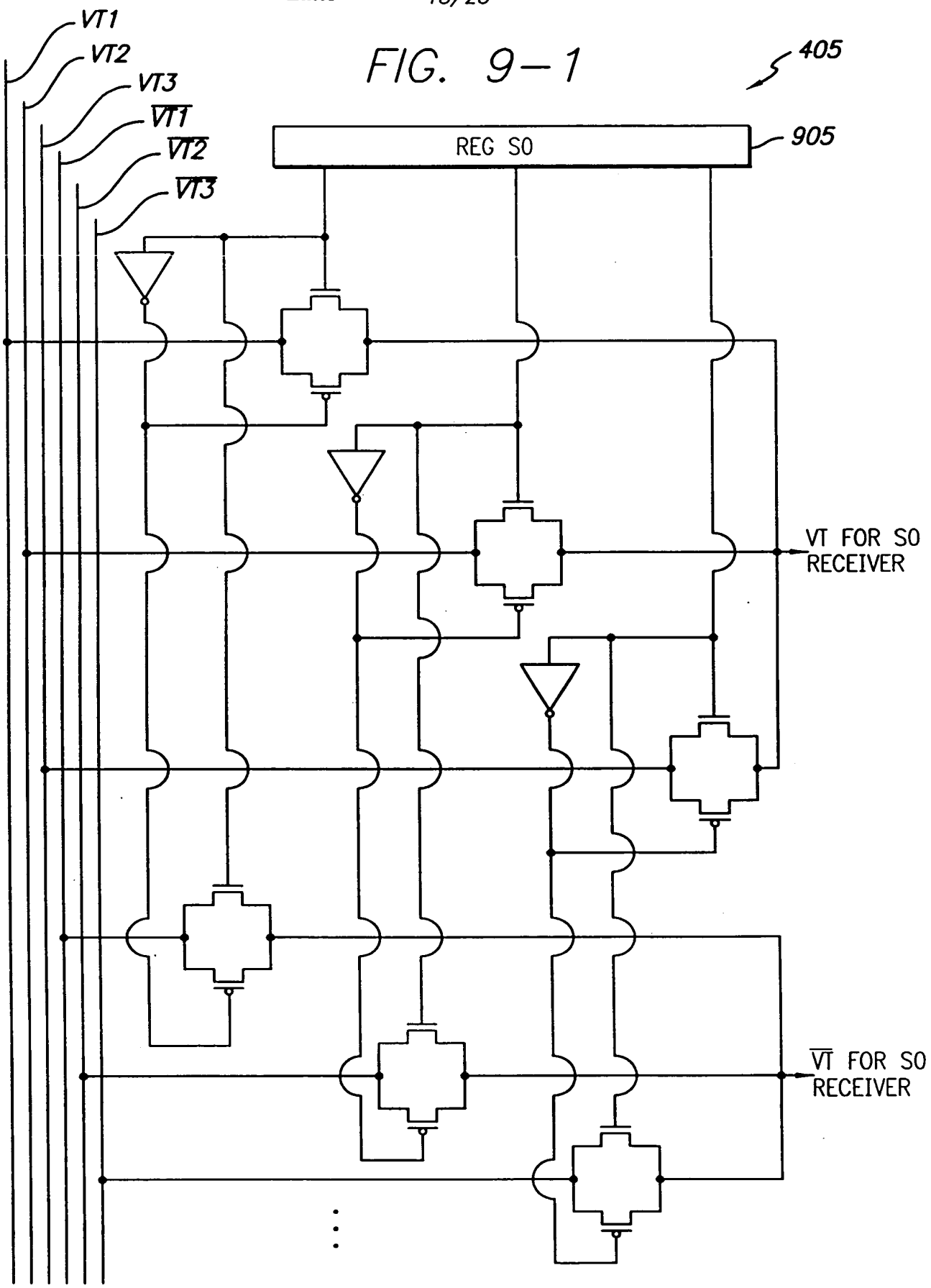

VT1
VT2
VT3
$\overline{VT1}$
$\overline{VT2}$
$\overline{VT3}$
405
REG S0
905
VT FOR S0 RECEIVER
$\overline{VT}$ FOR S0 RECEIVER

FIG. 9-2

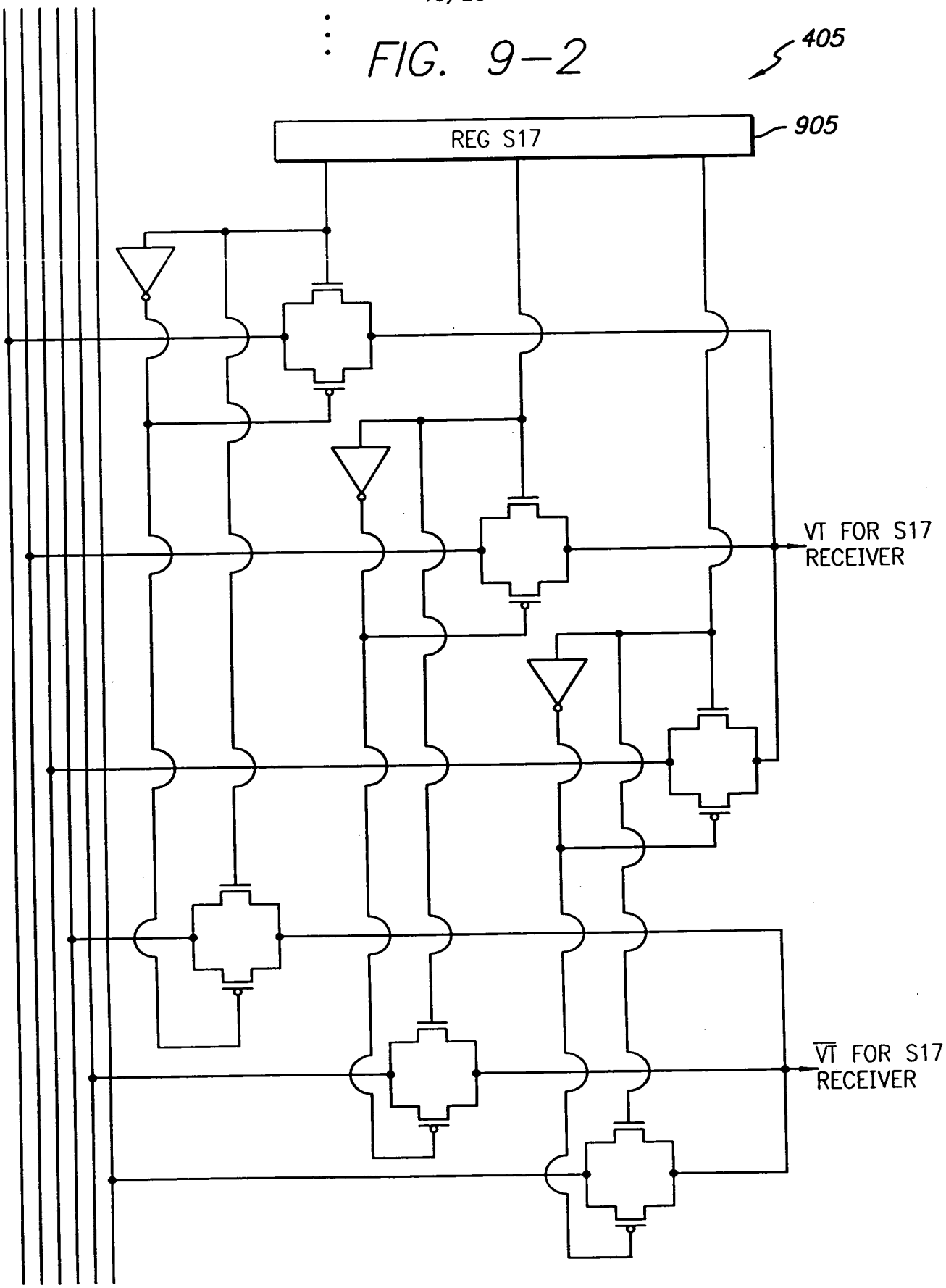
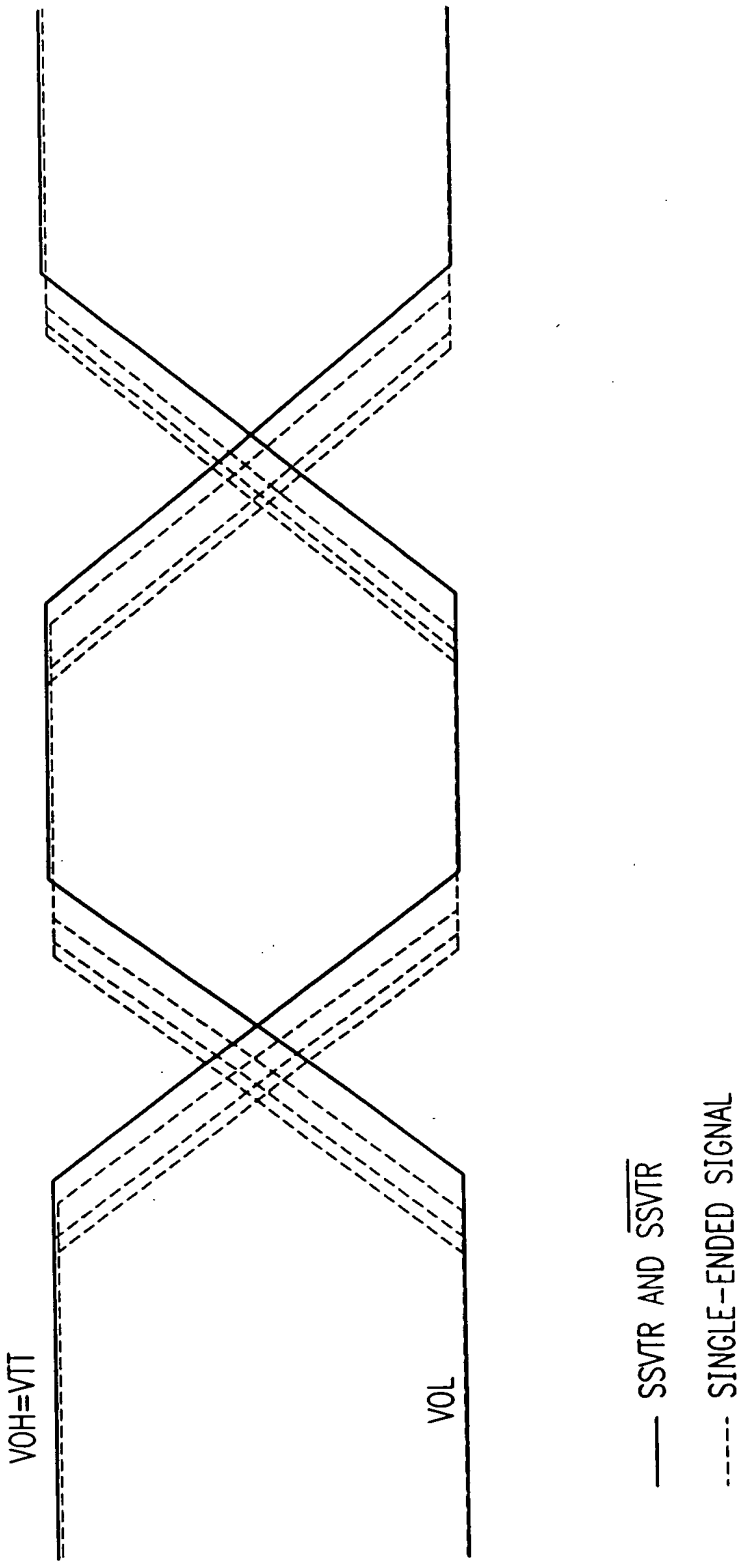

405
REG S17
905
VT FOR S17 RECEIVER
$\overline{VT}$ FOR S17 RECEIVER

FIG. 10



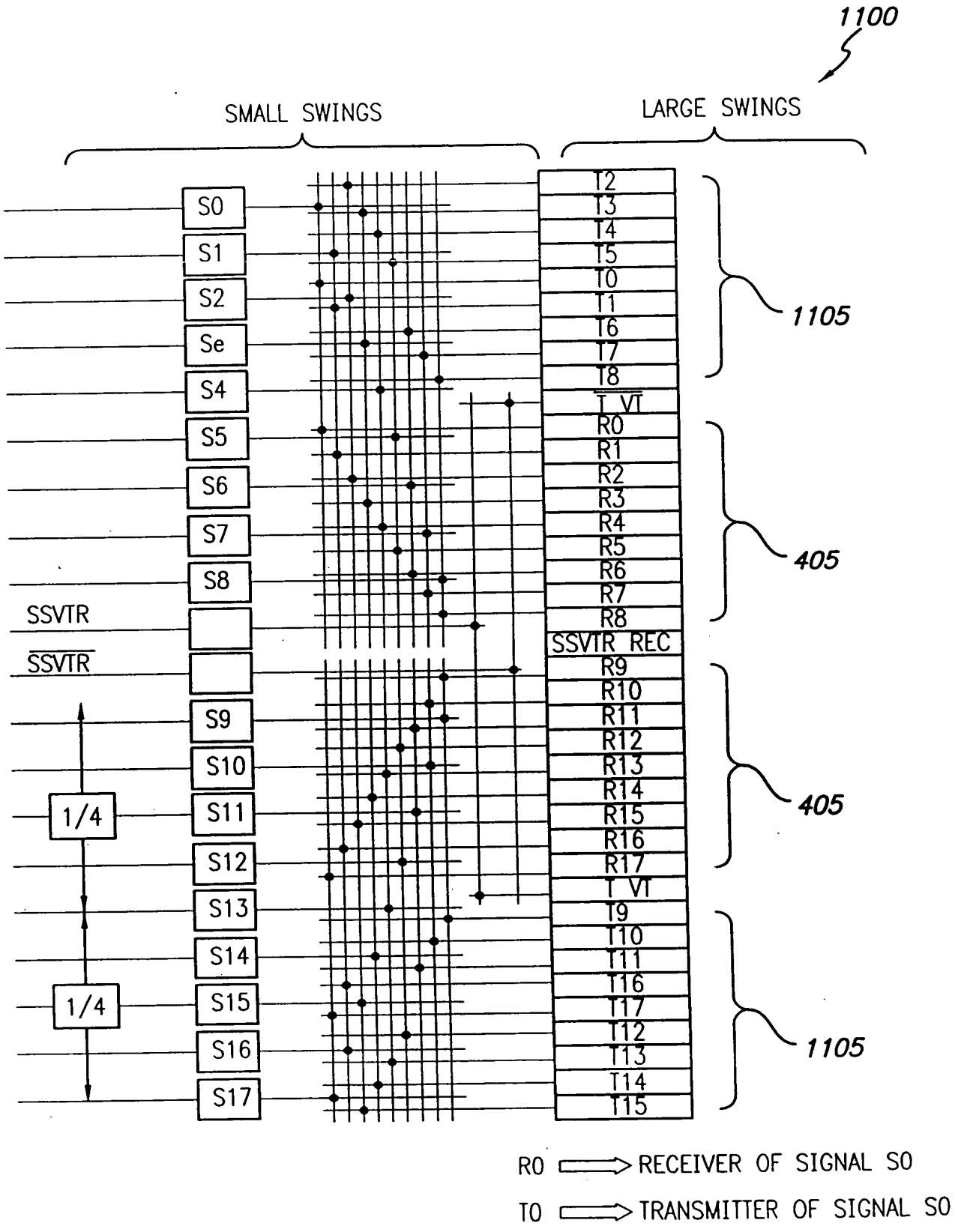

1100
SMALL SWINGS
LARGE SWINGS
S0
S1
S2
Se
S4
S5
S6
S7
S8
SSVTR
SSVTR
S9
S10
S11
S12
S13
S14
S15
S16
S17
1/4
1/4
T2
T3
T4
T5
T0
T1
T6
T7
T8
T VT
R0
R1
R2
R3
R4
R5
R6
R7
R8
SSVTR REC
R9
R10
R11
R12
R13
R14
R15
R16
R17
T VT
T9
T10
T11
T16
T17
T12
T13
T14
T15
1105
405
405
1105
R0 ⟹ RECEIVER OF SIGNAL S0
T0 ⟹ TRANSMITTER OF SIGNAL S0

FIG. 11

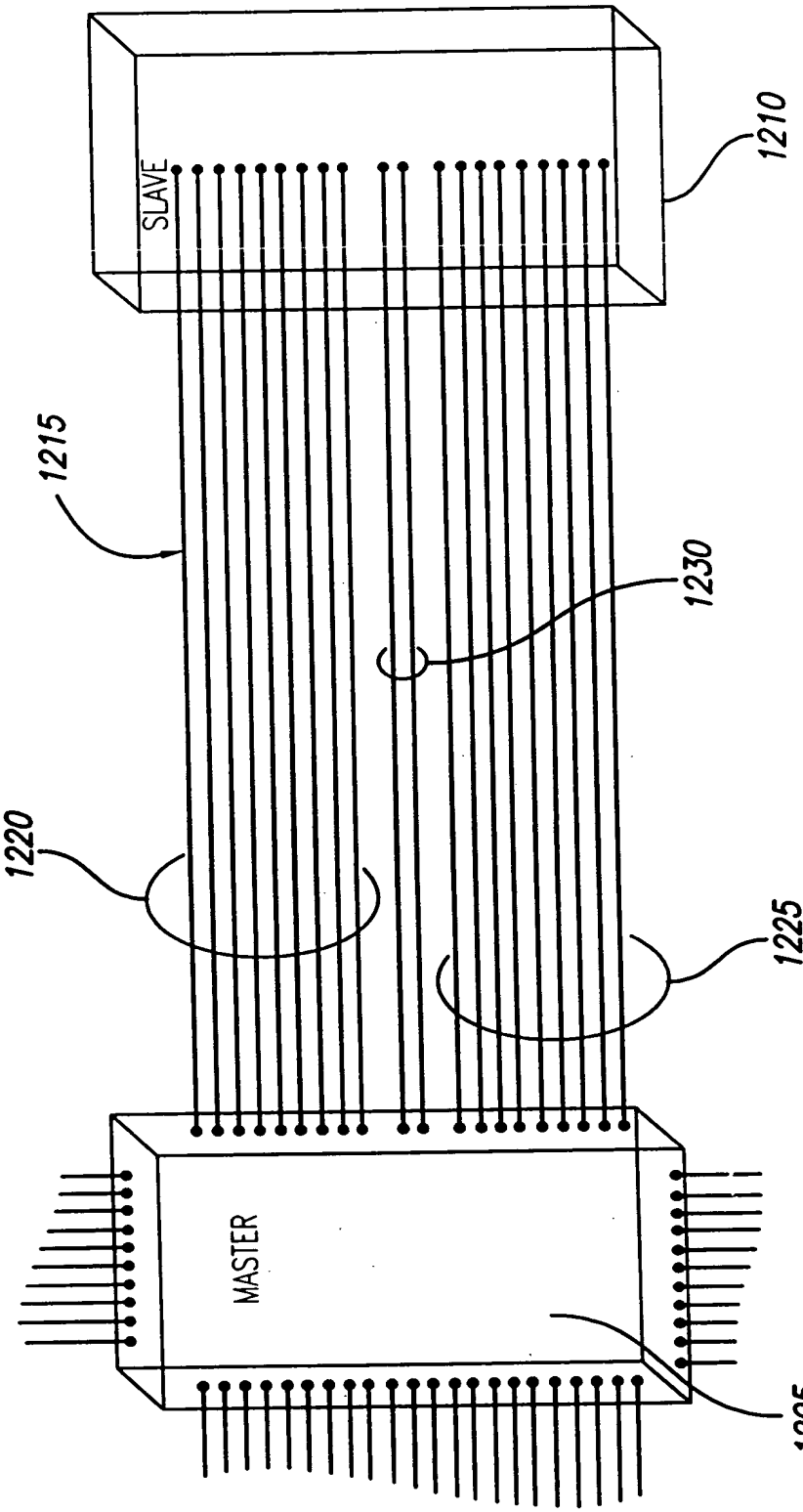


FIG. 12A

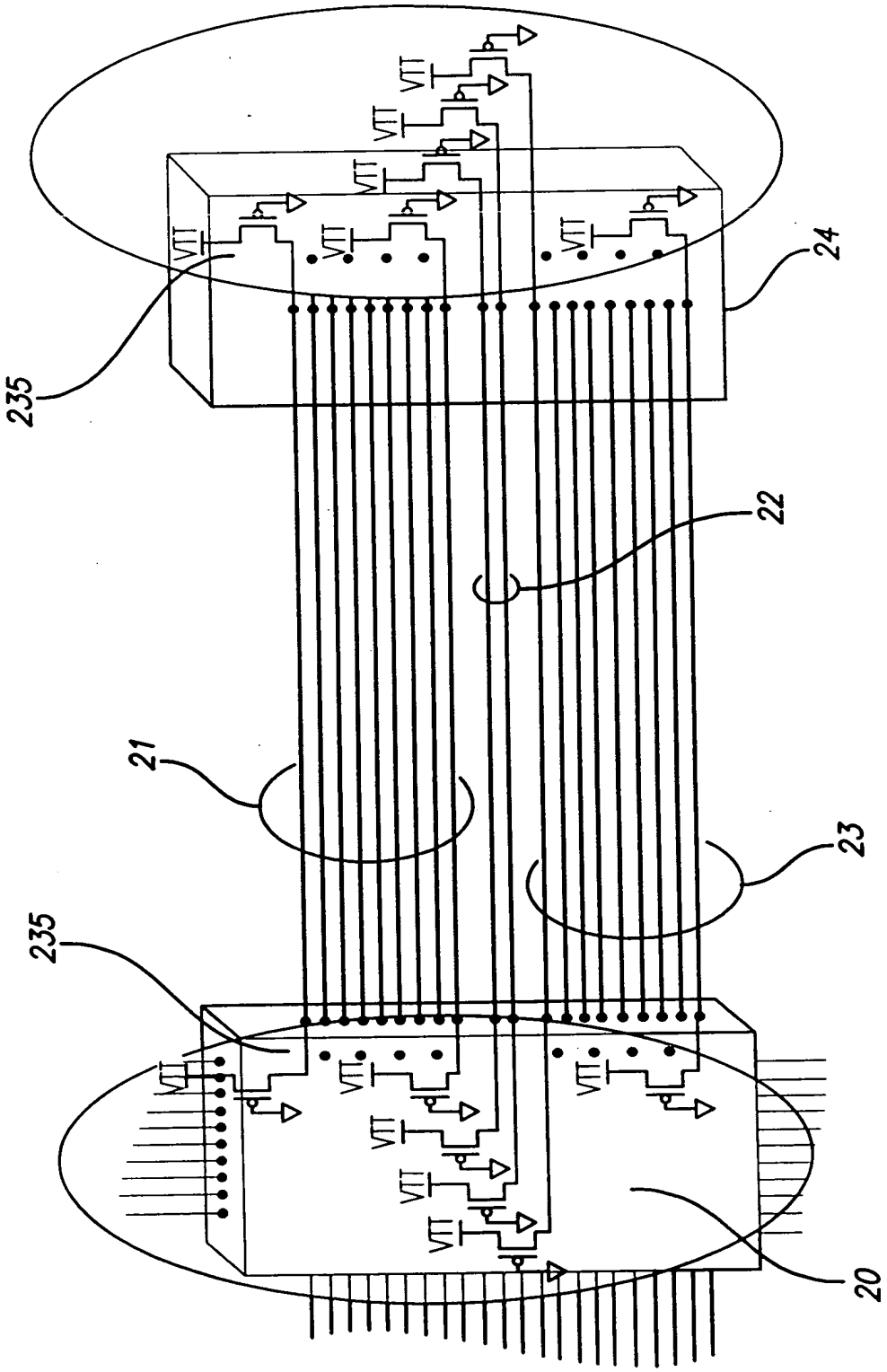


FIG. 12B

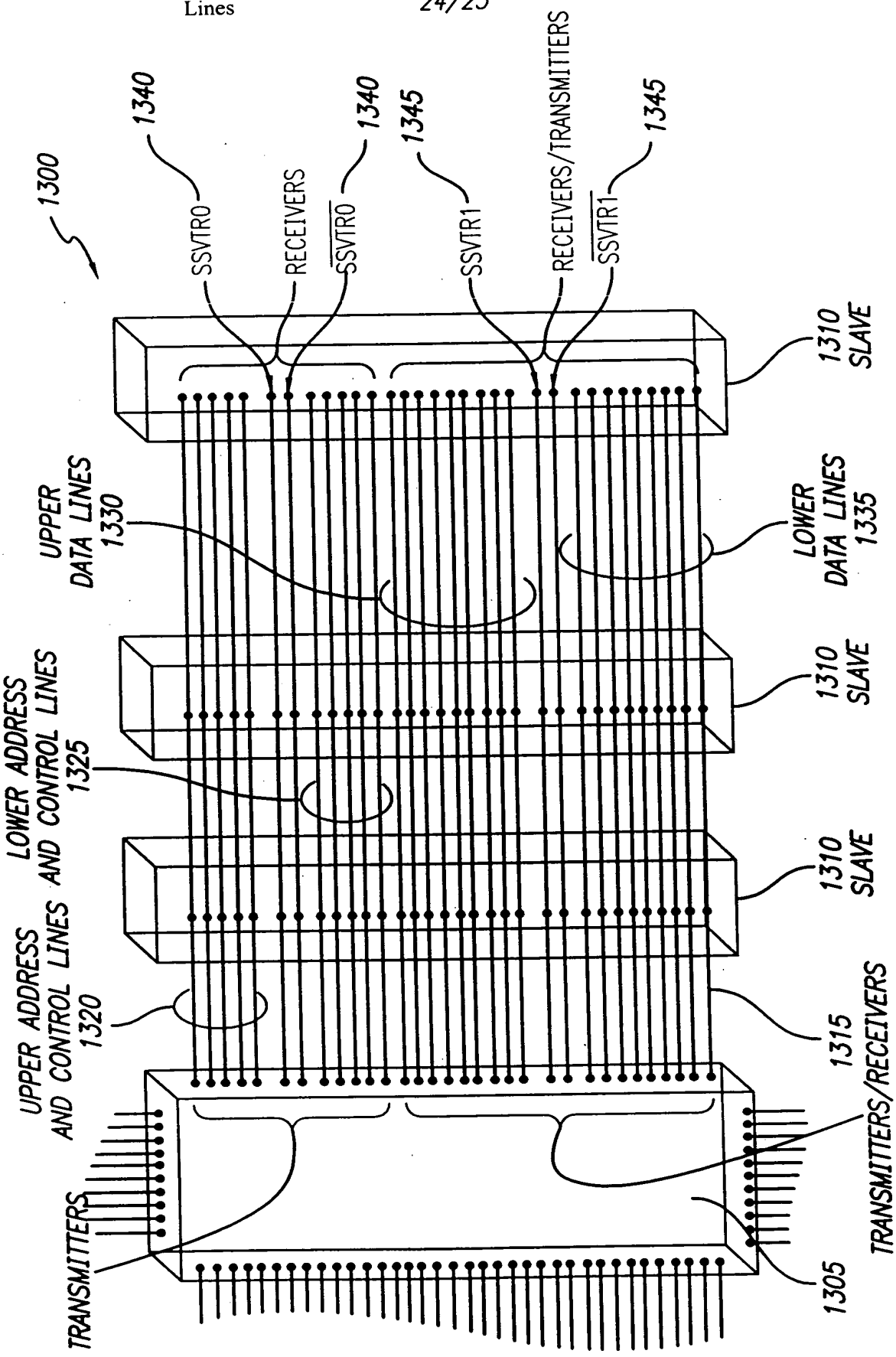

1300
1340
SSVTR0
RECEIVERS
1340
SSVTR0
1345
SSVTR1
RECEIVERS/TRANSMITTERS
1345
SSVTR1
1310 SLAVE
UPPER DATA LINES 1330
LOWER DATA LINES 1335
1310 SLAVE
LOWER ADDRESS AND CONTROL LINES 1325
1310 SLAVE
UPPER ADDRESS AND CONTROL LINES 1320
1315 TRANSMITTERS/RECEIVERS
TRANSMITTERS
1305

FIG. 13A

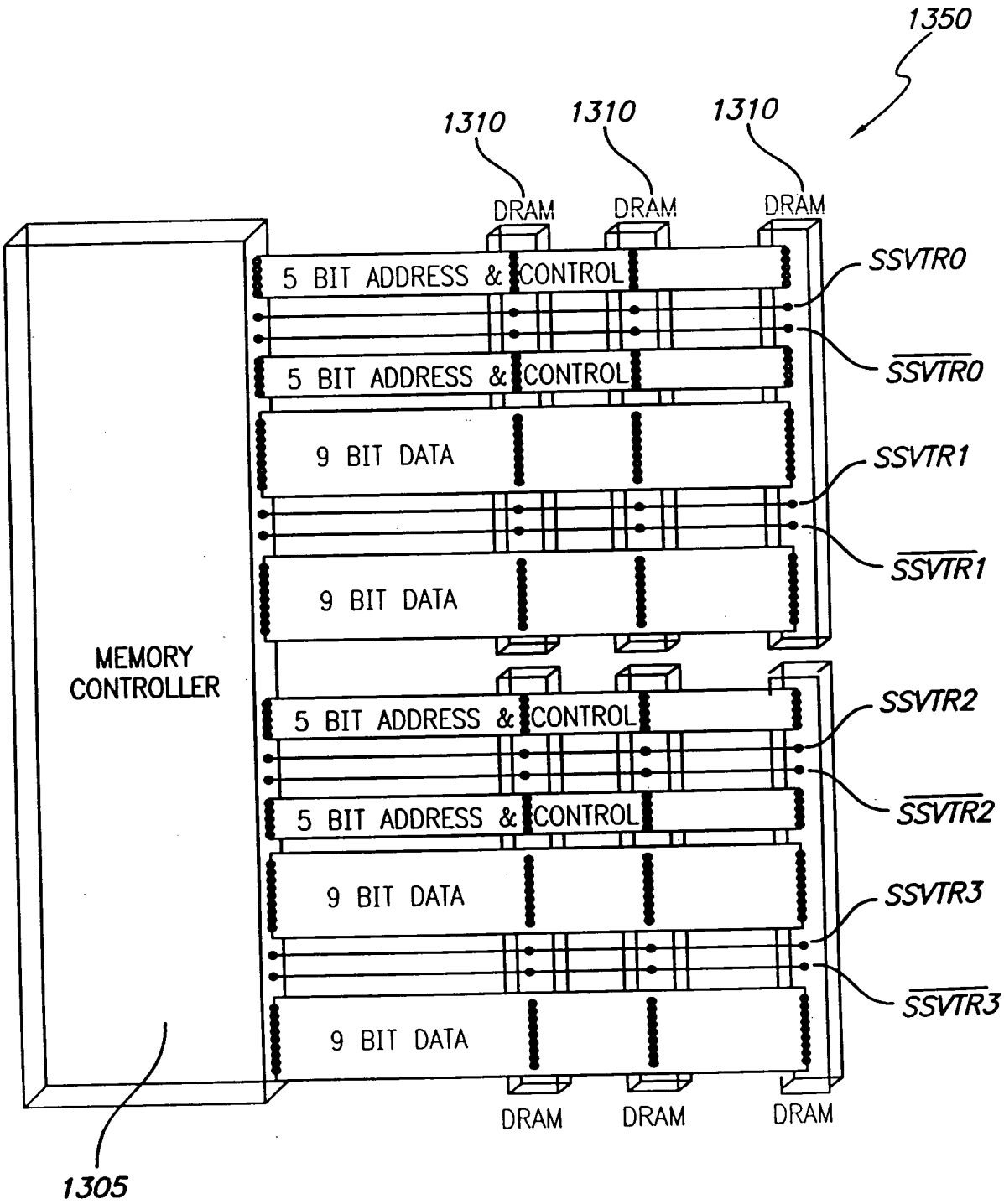

1350
1310
1310
1310
DRAM
DRAM
DRAM
5 BIT ADDRESS & CONTROL
5 BIT ADDRESS & CONTROL
9 BIT DATA
9 BIT DATA
5 BIT ADDRESS & CONTROL
5 BIT ADDRESS & CONTROL
9 BIT DATA
9 BIT DATA
SSVTR0
SSVTR0
SSVTR1
SSVTR1
SSVTR2
SSVTR2
SSVTR3
SSVTR3
MEMORY CONTROLLER
DRAM
DRAM
DRAM
1305

FIG. 13B